

3.304 Pico Boulevard/Santa Monica, California 90.405 USA P.O. Box 5339/Telephoné: (213) 450-2060/TWX: 910-343-6965

UNPACK AND SET-UP INSTRUCTIONS

IMPORTANT - Read This Before Unpacking

Both your Microcomputer Training System (MTS) and Interface Training System (ITS) are shipped to you completely assembled and tested. However, before operating your Training Systems, you should connect and test the various components to ensure that they have arrived intact. This process will also assist you in becoming familiar with the Training Systems and their accessories.

STEP 1 As you unpack, check off each of the items in the following packing list.

Packing List

Course 525, "Self-Study Microcomputer Software/

Hardware Training Course (MTS) (if included)

Qty	Stock No.	Description '	Check	Off
1	15605	Microcomputer Training System (modified)	() .
1	20032	Microcomputer Training System Workbook)
1	26001	Looseleaf Binder	()
1	26004	Coding Pad	()
		6, "Self-Study Microcomputer Interfa ining Course (ITS) (if included)	ce —	
1	15601-C	Interface Training System	()
1	20034	Microcomputer Interfacing Workbook	(`
-	20034	microcomputer interfacing workbook	(,
1	15606	ITS Experiment Kit (See Step 2)	()
1	26001	Looseleaf Binder	•),
1	15612	MTS/ITS Modification Kit (see step	3)()

STEP 2 Unpack the ITS Experiment Kit from the plastic bag and check off the parts from the following parts' list.

ITS EXPERIMENT KIT PARTS' LIST

			13.4	
Description	Stock No	, -	Qty.	V
Thermistor, disk, dipped in epoxy	15617		<u>. 1</u>	
Propeller, 5.5 x 4P	13616	2.5	g.g 1	
Motor, hobby, w/tinned lead wires	13617	2.44	49 1	
Speaker, w/tinned lead wires	15613		1	
Sleeve, motor shaft adapter, (piece of l inch long fuel line)	13619		91 1	
Cables, audio	15616		: - 2	
Resistor, 1K, 1/4 Watt, 5%	12608		10	
Wire, jumper, 8 inch lg., stripped	13621	:	· · · 4	
Program Cassette Library (One C-30 pre-recorded Cassette for Crs 536)	15614	- 51	1	
Capacitor, lmf, 15V, Electrolytic	12632	22.5	2 T 1	
Resistor, 10K, 1/4 Watt, 5%	12612	-	2	
Disk Wheel	13623		2 7 - 1	
Sensor, slot MCT8	15615		1	
Resistor, 180 Ohms, 1/4 Watt, 5%(Brn,Grey,Brn)	12616		1	_
Interconnecting Assembly	15602		1	
			e od	
	773381	2012		

STEP 3 If you ordered and received your Microcomputer Training System (Course 525) with the Interface Training System (Course 536), then you may skip this step and go on to Step 4.

If you ordered and received your MTS separately from the ITS, some modifications to the MTS may be required in order to operate the ITS. This modification is described in detail in the following pages (and in Appendix B of Course 536) and all required parts are included with this shipment (MTS/ITS Modification Kit). Comparing your MTS to the following illustrations, will determine if the modifications have already been accomplished. If the modification is required and you believe it to be beyond the electronic technician capability available to you, please return your unmodified MTS PC board with the MTS/ITS Modification Kit (stock number 15612) and a shipping label for its return to ICS at:

MTS Mods

Integrated Computer Systems, Inc.

3304 Pico Blvd.

P.O.Box 5339

Santa Monica, CA 90405

and we will install the modification free of charge and immediately return the modified MTS to you.

A CONTROL OF A SHEETING AND A CONTROL OF A C

•

In order to connect the Experiment Board (ITS) to the unmodified MTS board it is necessary to bring some additional signals from the MTS to the 100 Pin edge connector, P1. If you have the unmodified MTS board (part number 1052501-1) you may make these changes yourself. If you have the modified MTS (part number 1052501-1D) these changes are unnecessary.

a second modification is necessary to fix a potential problem. If your board is designated REV.E, this second modification is NOT necessary.

To modify the MTS, the following tools are required:

- 1) Low wattage soldering iron (20-40 watts)
- 2) Multi-core solder (Sn 60)
- 3) Wire strippers

ಕಾಗಿನ ವರಾತ್ರಗಳಿಂದ ಕುರ್ಕಾರ್ನಿಗಳ ಅವರ ಗುರ್ಕಾರ್ಟ್ ಕಾರ್ಗಿಸಿ

- 4) Wire cutters
- 5) X-acto knife or razor blade

The following parts are supplied in your MTS/ITS Modification Kit (Stock No. 15612)

- 1) 1 2n2222 transistor
- 2) 1 1K 1/4 watt resistor (Brown, Black, Red)
- 3) 1 10K 1/4 watt resistor (Brown, Black, Orange)

asion fautour die e al

- 4) 1 1n4148 Diode
- 5) 3 4 feet of jumper wire
- 6) Heat shrink tubing
- 7) 3 8.2 ½ watt resistors (Grey, Red, Red)

Flip the MTS board so that the solder side is face up and the keyboard mounting assembly is to your left. In Figure 1 , P1 is the 100 Pin edge connector. The "A" side corresponds to the pins on the component side of the board and is the set of plated through holes closest to the edge connector. The "B" side corresponds to the pins on the solder side of the board and is the second set of through holes from the edge connector pins.

The signals to be tapped (in "Board Designation" column of table 1 are marked on the component side of the MTS board. Follow the step-by-step procedure as outlined in table 1 and depicted in Figure 2.24

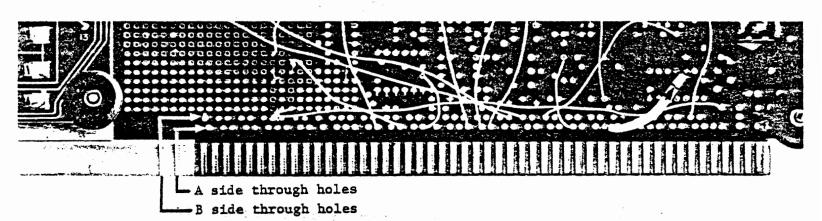


Figure 1
P1 100 Pin Edge Connector

STEP	CONNE From Board Designation	CTION To Edge Connector Designation Side/Pin	LENGTH OF JUMPER WIRE	(INCHES)
1	IOW	A35	3	
2	FOR	* A27	$3\frac{1}{4}$	
3	Ø ₂ (TTL)	- B7	3	
4	ŘESET 1	32 B20	2	
5 - 1	MEMR	A18	$1\frac{1}{4}$	
6	MEMW	A25	$3\frac{1}{2}$	and the same of th
7	INTR	A31	3 4	5
8	INTA	A26	3	V 15.
9	PCØ ²	B23	4	
10 *	PBØ ³	B22	5	

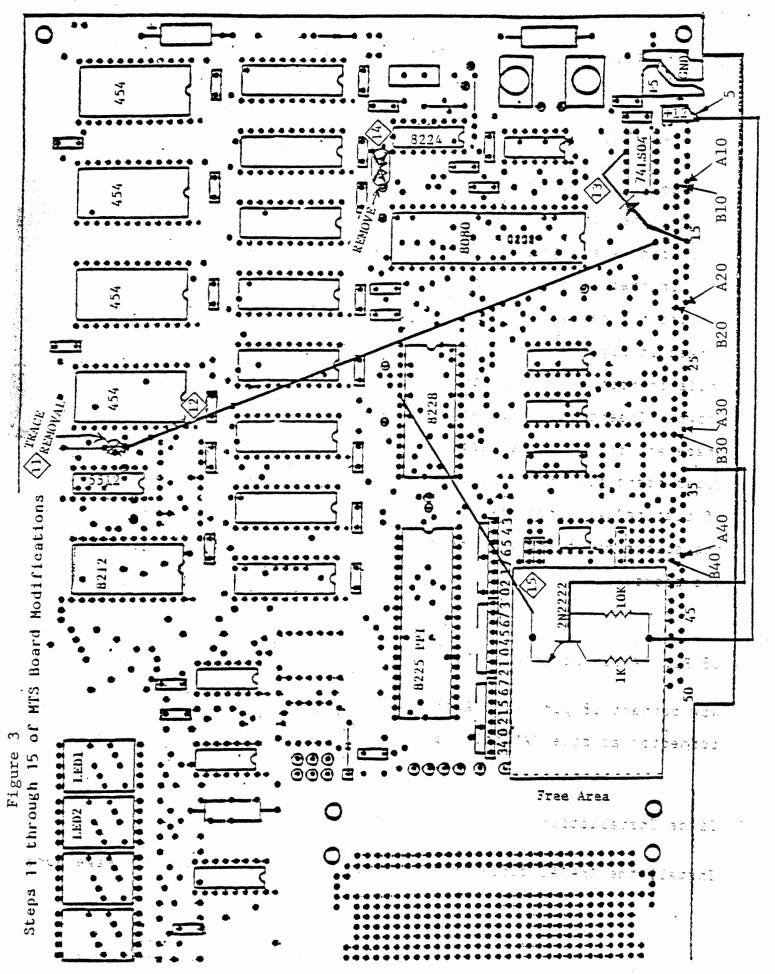
1 RESET Signal can be tapped from Ul (74LSØ4)

2 PC% is 8255 port C bit %

PBØ is 3255 port B bit Ø

Table 1

Steps 1-10 of MTS Modification



Refer to Figure 3 for the following steps.

11 Trace Removal

To allow for decoding of more memory, remove the trace between U8 (74155 chip) pin 14 and ground. A section of the printed circuit must be cut and removed between two solder points, as marked in Figure 4. Using the X-acto knife or razor blade cut the trace as shown. Insert the knife edge below the trace and pry up the edge from the fiber board backing. Now peel the line of plating away from the board up to the solder point and cut the trace from the board.

a marinima in the state of the

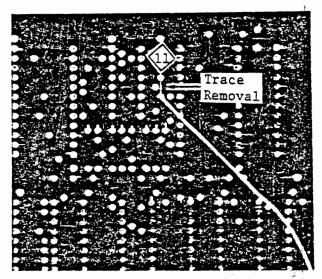


Figure 4
Trace Removal

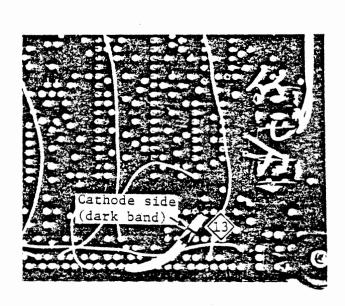
12 U8 Pin 14 to Address Bus 10~

Now connect U8 pin 14 to Address Bus 10 located on the 100 pin edge connector as side "A" hole 15 (P1-A15).

13 Diode Installation

Install the 1n4148 diode from U1 (74LSO4) pin 12 to P1-A15. Make sure

that the cathode side is towards U1 pin 12. The cathode side of the diode is marked with the dark band. Refer to Figures 5a and 5b for proper diode orientation. Insulate both ends of the diode with the heat shrink tubing. CAUTION: the tubing will shrink anytime heat is applied.



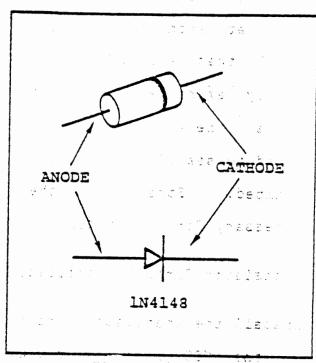


Figure 5a

Figure 5b

୍କିଲ୍ଲ ଓ ୧୯୯୬ - ୧୯୯୬ ଖର୍ମ ଓଡ଼ିଆ ଅନ୍ତର୍ଶ

or and sola rebu

Diode Orientation

14 Remove Resistor R62

Remove resistor R62 from the component side of the board as shown in Figure B-5. To remove R62, grasp the resistor from the component side of the board and heat each of the solder points until that end of the resistor is easily extracted. If the resistor binds, check the solder side of the board to see if the resistor leads are crimped. Straighten the leads if necessary for extraction.

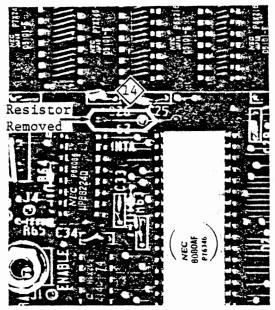
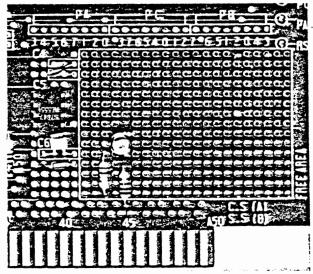


Figure 6
R62 Resistor Removal

Transistor Circuit Installation

Install the transistor circuit shown in Figure B-2b in the Free Area of the MTS board. A suggested parts layout is shown in Figures 7a and 7b. NOTE: The transistor and resistors are mounted on the component side of the board and the solder connections are made on the solder side of the board.



Suggested Parts Layout Component Side

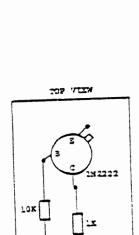
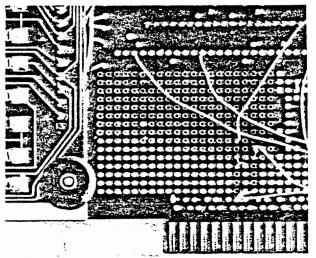


Figure 7a

Transistor Circuit

Component Side



Suggested Parts Layout Solder Side

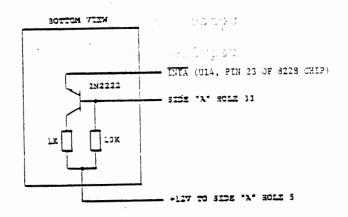


Figure 7b

Transistor Circuit

Solder Side

STEP 4 The MTS/ITS combination requires a greater capacity power supply than the MTS alone. If you have ordered and received a power supply from ICS of the following model numbers, please return it and we will immediately send to you a replacement of the required capacity:

XENTEK XM15-510

XENTEK XD114-512

All other power supplies provided by ICS have the required capacity.

Plug the ICS power supply in to a 115V AC source, then connect the output cable to the MTS board via the cable attached to lower left corner of the MTS circuit board. Proceed to Step 5.

If you did not purchase a power supply from ICS, then read the following discussion which describes the MTS/ITS power requirements. Note that these requirements are greater than those required for the MTS alone.

ICS MICROCOMPUTER TRAINING SYSTEM POWER REQUIREMENTS

The Microcomputer Training System is delivered as a ready-to-use unit requiring only connection of power supplies for operation. The MTS is designed to operate with only two DC power supplies, +12V and +5V. Among the parts used in the MTS, only the 8080A requires another supply voltage (-5V), which is generated internally.

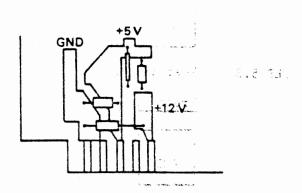
Both DC power supplies should have sufficient current margin over the following power dissipation specifications:

	_		÷	5₹	±	54	2.0	A	Max.
MI	S Power	Dissipation	+1	.2V	+	5%	1.0	A l	Max.

External power supply lines should be connected to the board edge finger pins marked +5V, +12V and GND.

The RS232c and TTY Interface circuits require -12V in some applications. This is discussed in Course 536, Appendix E.

Board Edge Finger Pins.



ICS MICROCOMPUTER TRAINING SYSTEM TEST PROCEDURE

STEP 5	Perform the ICS Microcomputer Training System Test	
	Modified MTS Board as detailed in the following page	es (reprinted from
	Course 525 Workbook, Appendix C).	
STEP 5.1	Set switches on left edge of board to "ENABLE" and "AUTO". LED's should display:	8200
STEP 5.2	Enter test program as follows by passing indicated keys :	
	Press Keys	Display Should be :
	MEM 2 1	8200 21
	NEXT 0 0	8201 00
	NEXT 8 4	8202 84
	Continue entering remainder of program from the following coding sheets (pages $\underline{19}$ and $\underline{20}$) from address 8203 to 8248 ⁺ . Once program has been entered, check to be sure that all instructions have been enetered correctly by pressing the keys:	
	RST NEXT NEXT etc.	
STEP 5.3	Test the RAM as follows :	
	Press Keys	Display Should be :
an com	ADDR	8200 21
	RUN	* 81FF

^{*(}IF YOU HAVE 1024 BYTES OF MEMORY THIS DISPLAY SHOULD BE 7FFF)

^{+ (}press the $\overline{\text{NEXT}}$ key after entering the data at 8248 so that 8249 is displayed in the LED's)

STEP 5.4 Test the ROM and keyboard as follows:

Press Keys	<u>Display Should be</u> :
0	145B 5D00
1	8E4C 2601
2	50DB F302
3	60BD 9903
4	04
5	05
6	06
7	07
8	08
9	

STEP 5.4 (cont'd)	Press Keys	Display Should be :
	A	OA
	В	OB
	С	, OC
	D	OD
an in the second	E	OE OE
Andrew Magnetic Consistence of the Consistence of t	F	OF
STEP 5.5	Test the command keys (excluding RST) as follows:	
	Press Keys	Display Should be :
enterphilippe (and the control of th	REG	
n gaptang at the original of t	MEM	10
Community (Special Professor Section 2)	BRK	<u> </u>
		17

STEP 5.5 (cont'd)	Press Keys	Display Should be :
	ADDR	12
	RUN	14
	STEP	13
	NEXT	15
	Repeat keys 0,1,2,3, and check previous list of displays for these keys.	
	The basic functions of the MTS are operational if all displays specified above have occurred during test sequence.	1 - 1440 1 - 1440
	Note : If the RAM test fails, try the ROM test by pressing the following sequence of keys :	
	Press Keys	
	RST ADDR 8 2 2	O RUN
		- Committee and the Committee of the Com
		e and page as come to
		er ja ja var var var var var var var var var va
		, the second contract of
		· · · · · · · · · · · · · · · · · · ·
per 1981 a		and the second s

	A	D	D	R	co	DE	RA	N	1		T-2	= 5	5 7	_				- 19 -
	8	2			ス			1	×	I		H	,	8	4	0	0	Address above highest
				1	0	0												memory location
				2	8	4												
}				3	1	1		4	×	ユ		A	`	8	2.	2	0	Address above test
lee T				4	2	0												program
3 SH				5	8	2_												•
CODING	8	- 2	0	6	1	\mathcal{P}		D	ح	R		تے						Decrement test
100				7	0	2		7	N	곧		8	2	0	د			program address
_				8	0	2												
				9	8	2_												
				Α	1	سكط		M	V	エ		E	٦	2	0			At 8200 set 8220
				В	2	0												
_	8	32	0	С	2	B		D	<u></u>	X		H						Decrement testaddress
SYSTEM				D	4	سے		M	0	1		C	_	M				Save memory data
.XS				E	1	A		4	D	4	X		4					Copy test program
				F	7	7		M	0	V		M	د	4				byte to memory
TRAINING	8	2	1	0	B	4		2	M			M						Test for success
RAI				1	2	2		J	N	2		8	2	1	A			Exit on error
ER T				2	1	A											·	
JTE	_			3	8	2												
CROCOMPUT				4	7	1		M	0	V		M		<u>ر</u>				Restore memory data
000				5	7	E		M	0	V		124	2	M				*
CRO				6	B	9		2	M	P		<u></u>						Test for success
Σ				7	0	A		J	7			8	2	0	6			Loop if OK
				8	0	6												•
				9	8	2					•							
S	8	2	1	Α	C	D		<u></u>	A	4	<u>_</u>		D	W	0	R	D	Exit - display location that could met be written
ΓEΝ				В	D	1												location that could
ΥS		<i>y</i> . ~ ·		С	0	2												met be written
 R.S		:		D	<u>C</u>	D		0	A	4	4		<u></u>	-6	R	G	7	
1		S.,		E	8													
MP	-			F	0	2												
$\frac{1}{2}$	8			0	<u> </u>													
TEC	_			1	-													
INTEGRATED COMPUTER SYSTEMS				2	_			CON	TIN	UEI	ON	TH	E N	EXT	PA	GE		
TEG				3	_													
Z	ļ			4	<u> </u>												-	
				5														
i				6	_											-		_
	<u> </u>			7														
	<u> </u>		·	8	<u> </u>													

8 2 Z 0 C D C A L L G E T K Y 1 3 D		A _D	0	R	coo	DE												
1 3 D 2 0 2 3 C D C A L L C L E A R 4 8 7 7 5 5 0 Z 6 C D C A L L D B Y T E 7 7 5 5 0 Z 7 7 9 5 8 0 Z 7 9 7 9 M O V A C A C C A C A C A C A C A C A C A C	1				_			C	A	L	1		2	E	T	K	Y	
2 0 2 3 CD CALL CLEAR 4 8 7 5 0 2 6 CD CALL DBYTE 7 9 5 3 0 2 9 79 MOV A, C A FE CPT O H 8 0 4 C D Z JNC 82 2 0 DISPLAY ADDRESS F DS P USH D DISPLAY ADDRESS 8 2 3 0 5 1 MOV D, C HIGH ADDRESS KEY CLEAR LOW ADDRESS 8 2 3 0 5 1 MOV E, A CLEAR LOW ADDRESS 1 A F X R A A CLEAR LOW ADDRESS 2 3 F MOV E, A CLEAR FOR AOD 4 6 F MOV L, A SUM 5 4 7 MOV B, A CLEAR FOR AOD 6 E B X CH G 7 4 E MOV C, M GET BYTE 8 E B X CH G 9 0 9 D A D B ADDRESS 7 4 7 MOV C, M GET BYTE 8 E B X CH G 9 0 9 D A D B ADDRESS 1 A A 9 X R A C FORM LRC 1 D R P B 2 3 5 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L D D BY Z 1 D C A L L D BY Z				1		+												
3 CD CALL CLEAR R 4 87 5 02 6 CD CALL DBYTE 7 95 8 02 9 79 MOV A, C A FE CPI OH C D2 JNC 8220 E 82 F D5 PUSH D DISPLAY ADDRESS 8 2 3 0 5 I MOV D, C HIGH ADDRESS KEY C D2 JNC B2 ZO E 8 2 F D5 PUSH D CLEAR LOW ADDRESS 3 G7 MOV E, A CLEAR LOW ADDRESS 3 G7 MOV E, A CLEAR ARITHMETIC 4 GF MOV L A SUM 5 4 7 MOV B, A CLEAR FOR ADD 6 EB X CH G 7 HE MOV C, M GET BYTE 8 E B X CH G 9 0 9 D AD B A CHEAR FOR ADDRESS 2 C C Z JNZ 8 2 3 5 E 8 2 F D1 POP D DISPLAY ADDRESS C C C Z JNZ 8 2 3 5 C C C Z JNZ 8 2 3 5 C C C Z JNZ 8 2 3 5 C C C Z JNZ 8 2 3 5 C C C C Z JNZ 8 2 3 5 C C C Z JNZ 8 2 3 5				2	-	+												
4 8 7 5 0 2 6 C D C A L L D B Y T E 7 9 5 8 0 2 9 7 9 M O V A C A F E C P I O Y B 0 Y D D DISPLAY ADDRESS 8 2 7 1 A F E X R A A CLEAR LAC LOCAR AKITHMETIC 2 5 F M O V E A CLEAR LOCAR AKITHMETIC 4 6 F M O V B A CLEAR FOR ADDRESS 5 4 7 M O V B A CLEAR FOR ADDRESS 7 4 E M O V C M CET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B AD BYTE FORM LRC 1 D R P O P D DISPLAY ADDRESS 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE FORM LRC 1 D R P O P D DISPLAY ADDRESS 1 D C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C Z J N Z 8 2 3 5 1 D C C C C C C C C C C C C C C C C C C				3		1		1	A	L	L	(-	L	E	A	R	
6 C D C A L L D B Y T E 7 9 5 8 0 2 9 7 7 9 M O V A, C A F E C P I O H 8 0 H C D Z JN C 82 Z O D Z O D Z O D C D C HIGH ADDRESS 1 A F X R A A CLEAR LOW ADDRESS 1 A F X R A A CLEAR LOW ADDRESS 3 G 7 M O V E, A CLEAR LOW ADDRESS 3 G 7 M O V E, A CLEAR ARITHMETIC 4 G F M O V E, A CLEAR ARITHMETIC 4 G F M O V E, A CLEAR FOR AOD 6 E B X C H G SUM 7 H E M O V C, M GET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE FORM LRC 1 N R E TUCK ADDRESS 0 3 5 T N R 8 Z 3 5 0 3 5 T N R 8 Z 3 5 1 9 8 Z 1 9 7 Z O D D D D DISPLAY ADDRESS 1 9 O P D D D DISPLAY ADDRESS 1 1 N R E TUCK ADDRESS 1 9 O P D D D DISPLAY ADDRESS	EE			4		+												
6 C D C A L L D B Y T E 7 9 5 8 0 2 9 7 9 M				5	_	_												
9 779 M Q V A, C A F E C P I O 4 B O 4 C D 2 JN C 82 2 0 E 8 2 F D 5 P U S H D DISPLAY ADDRESS B 2 3 0 5 1 M Q V D, C HIGH ADDRESS = KEY I A F X R A A A 2 5 F M Q V E A CLEAR LRC 2 5 F M Q V E A CLEAR LOW ADDRESS 3 G 7 M Q V H A CLEAR RITHMETIC 4 G F M Q V L A SUM 5 4 7 M Q V B A CLEAR FOR AOD 6 E B X C H G ADDRESS RAM 7 4 E M Q V C, M GET EYTE 8 E B X C H G SUM DE SUM 7 4 E M Q V C, M GET EYTE 8 B B X C H G SUM DE SUM 8 C C C Z JN Z 8 2 3 5 D 3 5 C C C Z JN Z 8 2 3 5 D 3 5 D DISPLAY ADDRESS 9 0 9 D A D B ADD BYTE FORM LRC 1 N R E J DISPLAY ADDRESS 1 9 8 2 5 D DISPLAY ADDRESS 1 9 8 2 6 C 3 JM P 8 2 2 0 6 C 3 JM P 8 2 2 0 7 2 0 JM P 8 2 2 0 8 2 JM P 8 2 2 0 9 3 JM				6		+		1	A	_	L	r	o	B	۲	T	F	
9 779 M Q V A, C A F E C P I O 4 B O 4 C D 2 JN C 82 2 0 E 8 2 F D 5 P U S H D DISPLAY ADDRESS B 2 3 0 5 1 M Q V D, C HIGH ADDRESS = KEY I A F X R A A A 2 5 F M Q V E A CLEAR LRC 2 5 F M Q V E A CLEAR LOW ADDRESS 3 G 7 M Q V H A CLEAR RITHMETIC 4 G F M Q V L A SUM 5 4 7 M Q V B A CLEAR FOR AOD 6 E B X C H G ADDRESS RAM 7 4 E M Q V C, M GET EYTE 8 E B X C H G SUM DE SUM 7 4 E M Q V C, M GET EYTE 8 B B X C H G SUM DE SUM 8 C C C Z JN Z 8 2 3 5 D 3 5 C C C Z JN Z 8 2 3 5 D 3 5 D DISPLAY ADDRESS 9 0 9 D A D B ADD BYTE FORM LRC 1 N R E J DISPLAY ADDRESS 1 9 8 2 5 D DISPLAY ADDRESS 1 9 8 2 6 C 3 JM P 8 2 2 0 6 C 3 JM P 8 2 2 0 7 2 0 JM P 8 2 2 0 8 2 JM P 8 2 2 0 9 3 JM													+		-			
9 79 M Ø V A C A F E C P I O 4 B O 4 C D Z J N C 82 Z O E 8 Z F D 5 P U S H D DISPLAY ADDRESS 1 A F X K A A C CLEAR LRC 2 5 F M Ø V E A CLEAR ARITHMETIC 4 6 F M Ø V L A SUM 5 4 7 M Ø V L A SUM 6 E B X C H G ADDRESS RAM 7 4 E M Ø V C M GET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE A A 9 X K A C FORM LRC 1 N R E TUCK ADDRESS C C Z J N Z 8 Z 3 5 E 8 Z 1 F D 1 P Ø P D D DISPLAY ADDRESS 3 Z 4 0 C D C A L L D B Y Z 6 C 3 J M P 8 Z Z O	7				-	+							7					
A F E C P I O 4 8 0 4 C D 2 JN C 82 2 0 E 8 2 F D 5 P U S H D DISPLAY ADDRESS 8 2 3 0 5 1 M V D C CLEAR LOW ADDRESS 3 6 7 M V H A CLEAR ARITHMETIC 4 6 F M V L A SUM 5 4 7 M V L A SUM 6 E B X C H G ADDRESS RAM 7 4 E M V C M CET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE A A 9 X R A C FORM LRC 1 N R E TWCR ADDRESS C C 2 JN Z 8 2 3 5 D 3 5 D DISPLAY ADDRESS 8 2 4 0 C D C A L L D B Y Z 6 C 3 JM P 8 2 2 0 7 2 0	-					+		M	0	V	1		A					
B 0 4						+					+		7	4				
C D 2 JNC 8220 D 20 DISPLAY ADDRESS F DS PUSH D DISPLAY ADDRESS 8 2 3 0 5 1 MOV D, C HIGH ADDRESS FEY 1 A F X R A A CLEAR LAC 2 S F MOV E, A CLEAR ARITHMETIC 4 G F MOV L, A SUM 5 4 7 MOV B, A CLEAR FOR ADDRESS 6 E B X C H G ADDRESS RAM 7 4 E MOV C, M GET BYTE 8 E B X C H G Sum TO HL 9 0 9 D A D B ADD BYTE A A 9 X R A C FORM LRC 8 1 C I N R E TUCK ADDRESS C C 2 J N Z 8 2 3 5 D S 2 4 0 C D C A L L D B Y Z 6 C 3 J M P 8 2 Z 0 7 2 0						+		-	 				-					
E 8 2	-					+		17	12	1		(2	2	2	0		
S	Σ					+		1	11-	-		-	-	-	-			
S	SIE				-	+		-		 			+				-	
8 Z 3 0 5 1 M V D , C HIGH ADDRESS = KEY 1 A F					-	_		0	11	15	H		5		1		—	DISPLAY ADDRESS
3 6 7 M O V H, A CLEAR ARITHMETIC 4 6 F M O V L, A SUM 5 4 7 M O V B, A CLEAR FOR ADD 6 E B X C H G ADDRESS RAM 7 4 E M O V C, M CET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE A A A 9 X R A C FORM LRC TOUR ADDRESS C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C C C C C C C C C C C C C C C C C	됩는	R Z	3								-			<u> </u>	1			
3 6 7 M O V H, A CLEAR ARITHMETIC 4 6 F M O V L, A SUM 5 4 7 M O V B, A CLEAR FOR ADD 6 E B X C H G ADDRESS RAM 7 4 E M O V C, M CET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE A A A 9 X R A C FORM LRC TOUR ADDRESS C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C C C C C C C C C C C C C C C C C	3				_	11		1			_		_	1	_		-	
3 6 7 M O V H, A CLEAR ARITHMETIC 4 6 F M O V L, A SUM 5 4 7 M O V B, A CLEAR FOR ADD 6 E B X C H G ADDRESS RAM 7 4 E M O V C, M CET BYTE 8 E B X C H G SUM TO HL 9 0 9 D A D B ADD BYTE A A A 9 X R A C FORM LRC TOUR ADDRESS C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C 2 J N Z 8 2 3 5 C C C C C C C C C C C C C C C C C C C								1	1		,	-	-		A		-	
8 E B					-			7		1							-	
8 E B	計				_	+		-	1 1,	_	-	+++	1	لرا	_	-	-	
8 E B	JM-				_		-		11			- 4	=)	1	-	-	
8 E B	3 -					+	-					- 	ېک	 \	A	-	-	
8 E B	하				_	_		1		_	_		_	-	-	-	+-	
9 0 9 D A D B ADD BYTE A A 9 XR A C FORM LRC B 1 C INR E THOR ADDRESS C C 2 JNZ 8 2 3 5 D 3 5 D D D D D D D D D D D D D D D D D	<u> </u>							Τ.	10	14	+	+	اك	لرا	M	-	+	
A A 9 XR A C FORM LRC B 1/C INR E TWCR ADDRESS C C Z JNZ 8 2 3 5 D 3 5 E 8 2 F DI P P P D DISPLAY ADDRESS 8 2 4 0 C D C A L L D B Y Z 1 9 8 2 0 2 3 C D C A L L D W D Z 4 D 4 5 0 2 7 2 0 7 2 0	L						-						_		-	-	-	
B	-							-	_	_	_			-	-	-	+	i i
5 0 2 6 C 3 JHP 8220 7 20	SI				1	+							$\overline{}$		 '	-	+	1
5 0 2 6 C 3 JHP 8220 7 20	LEN				11									_	2	+	_	TUCK ADDRESS
5 0 2 6 C 3 JHP 8220 7 20	XX.							12	N	Z	-	+	<u>ර</u>	4	13	15	-	
5 0 2 6 C 3 JHP 8220 7 20	RS							+	+-	4		+-+		4	 	-	-	·
5 0 2 6 C 3 JHP 8220 7 20	라							广	+	+_		++	$\overline{}$	<u> </u>	<u> </u>	-	+-	
5 0 2 6 C 3 JHP 8220 7 20	MP.										+		-	-	1	-		DISPLAY ADDRESS
5 0 2 6 C 3 JHP 8220 7 20	3/2	8 2	4					1	A	1	1	4	<u>D</u>	B	Y	Z		
5 0 2 6 C 3 JHP 8220 7 20	ED					1	1 ′					4-+		1	_ '	-	_	
5 0 2 6 C 3 JHP 8220 7 20	RAI								1					1	'			
5 0 2 6 C 3 JHP 8220 7 20	EG			3	C	-		<u> </u> C	A	L	L		<u>D</u>	W	D	2		
5 0 2 6 C 3 JHP 8220 7 20	Z																	
7 20				5														
						-		J	M	P			8	2	Z	0		
3 2				7									1					
				3	7.3	2												

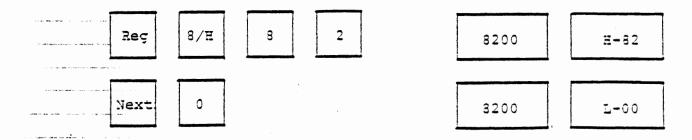
STEP 6 Unplug MTS board from power supply.

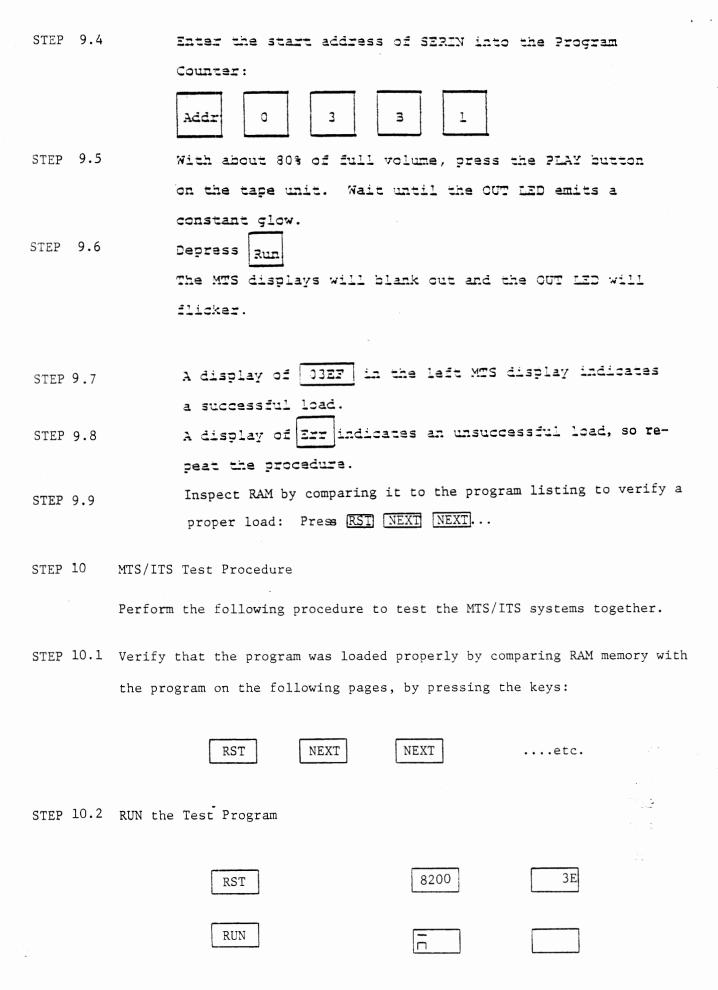
STEP 7 MTS to ITS Connector.

The adaptor circuit board via its connector is plugged into the MTS, with the ribbon cable running under the MTS and folded to come out to the left, as shown in Course 536 Workbook Figure 1-1. The cable is plugged into the connector at the right hand side of the interface board. Make this connection.

- STEP 8 Plug in the power supply (see Step 3) and then connect it to the MTS board via the cable at the lower left corner of the MTS circuit board.
- STEP 9 Load MTS/ITS Test Program

 Perform the following procedure to load the MTS/ITS Program from the
 Program Cassette Library.
- STEP 9.1 Find the test program on the Cassette Library tape and listen for the solid tone which PRECEDES the program.
- STEP 9.2 Connect the cable to EAR on the tape unit and CASSETTE EAR (screw terminal #7) on the ITS board.
- STEP 9.3 Enter the beginning load address into Reg Pair H. The beginning address of the test routine is 8200:





3TEP 10.3 The 8 ITS LED's and MTS 7-segment LED's should alternately display at a 4 second blink rate:

AND THEN DISPLAY

This test exercised the interrupt system and one of the 8253 timers (Timer 0) as well as the connector cable.

STEP 11 If the tests were successful, then proceed with the appropriate workbook.

> If the tests give questionable results, perform the following diagnostic procedure. If your board still malfunctions, call us at (213) 450-2060.

ICS warrantees its hardware for 90 days from date of delivery against defects in material or workmanship.

STEP 12 MTS/ITS Diagnostic Procedure

Test No. I Symptom Possible Cause Possible Fix 8200 does not Poor Ribbon Cable Contact 1) Turn power off appear in MTS 2) Disconnect ribbon cable at MTS display

- 3) Power on, Press RST
- 4) If 8200 now appears, check ribbon connector (Test Number III) or ITS.
- 5) If 8200 does not appear, check powersupply (test No. II) or MTS.

Test No. II Symptom Possible Cause Possible Fix MTS operation erratic Insufficient Power 1) With MTS and ITS connected and powered up, check the voltage MTS display flickers levels: or flashes 2) 5V supply must provide at least 4.80 volts. RAM memory changes 3) 12V supply must provide at least 11.5 volts Test No. III 8 LED's at top left Reversed Ribbon Cable 1) Turn power off corner of ITS are all off Ribbon cable at ITS connector must have colored edge stripe towards the top of board 3) Ribbon cable at MTS connector must leave small printed circuit board under the MTS 4) Compare ribbon cable connectors with Course 536 workbook figure 1-1 1) Connect a wire between CASSETTE Oxide buildup on MTS AUX AND CASSETTE EAR on barrier edge connector strip on ITS board 2) With power on, the "OUT" LED should glow with full brilliance, and the SYM light should glow at less than full brilliance 3) Depress the following sequence of keys: RST REG 0 NEXT 0 NEXT NEXT REG D 0

3

0

ADDR

7

5

RUN

	MTS/	T T	5	Ju	MO	11.2	Ţ.			ΪŅ	vite;	rtão	3	Tes	Routine C/8/78
						÷									
		a	u+	hor.	M.	۲.	Mi	33,L 176	, 4	i iĝ.	, v (·				
8	5 Q 0	3	3		M	Y	I		A	,	8	0			INItialize 8255's
	1	8	Ø							,					
	2	D	3		0	4	T	,	7	Ν	7	1			#1 is all out
	3	Ø	7												
	4	3	ε		M	V	I		A	,	3	2			# 2 15 A-0UT
	5	3	2							,					B - 10
	6	D	3		0	ч	T		c	N	T	2			C-047
	7	Ø	F												
	8	3	3		M	V	I		4	,	3	Ø			Initialize Timer O
	9	3	Ø							/					·
	Α	D	3		0	4	T	·	7	1	17	(T		
	В	1	7												
	С	3	ε		M	V	I	1	2		Ø	1			and enable its interrupt
	D	Ø	1							1		•			
	E	D	3		0	u	17		2	N/	7	2.			
	· F	Ø	=												
8	210	3	3		M	V	I		4	,	5	5			Output Pattern 1:
	1	5	5							,					(01010101)
	2 ·	D	3		0	u	T	1	P	0	R	T	1	Α	To LED'S
-	3	Ø	4												
	4	3	2		<	T	A		8	3	F	Ω,			and Display
	5	F	8			<u> </u>	1			_					
	6	8	3						1						
	7	D	3		0	u	-		, 	1	M	2			Reload Timer of
	8	1	4		Ť							<i>*</i>			
	9	D	3		0	u.	7	-	7	I	1-1	Ø			
	A	1	4												
	В	5	7		M	0	V				A				Save Pattern
	G	Ø	6		14	٧	I		B	1	3	2			Initialize 2 winter
	D	3	2							,					
	E	4	8		M	0	V	1 (1		\mathcal{B}				Save Country
1	21 F	c	3.	WAIT	7	M	p	-	_	A.	I	T			Wait for Internet
8	0	1	E		Ť				1	` '		,			
8	1	8	2												
	2	Ť													

Test No. III, Cont'd

Symptom

Possible Cause

Possible Fix

- 4) The "OUT" LED should blink rapidly for several seconds, after which it will glow brightly. Meanwhile, the SYM light should glow steadily at about half brilliance. This indicates that the cassette interface is functioning properly
- 5) If the OUT and SYM LED's don't behave, as in #4 above during a cassette load, then your cassette connections may be incorrect. Follow the instructions in Course 536 workbook, Appendix D and compare the cassette interface connections with the photo in Appendix D.

	~ , ·			· · · · · · · · · · · · · · · · · · ·														<u> </u>
				MT	5,	/I	75	// J	UM	ጉ <i>ነ</i>	10	JA	ck	!!	IN	ito	yyu	pt. Service Poutine
										,	V							
	8		/	0									, i *			/		
				1										/				
				2			/						/					
_[3		,					1							
빌				4	/					/								
				5 🦯				/								/		
				6										, ,				
CODING SHEET				7														
	8	, 5	2	8	Ø	5		D	C	R		B						Decrement Counter
				9	C	2		7	N	7		I	N	I	Τ			Not time yet
				A	3	5												, ·
				В	8	5	٠.											
				C	7	A		M	0	V		A	,	D				Now's the time:
EH I HAINING SYSTEM				D	2	F		C	14	A			Í		•			Reverse sense of
2				E	5	7		M	0	V		D		A				bits and
2				F	D	3		0	u	7		P	Ô	R	T	1	A	cutput NEW fortern
	8	2	3	0	Ø	4-												to LED's
				1	3	2		5	T	A		8	3	F	8			and Display
				2	F	18												·
				3	8	3							,					
				4	4	1		M	0	V		B		C				Reload Counter
MICHOCOMPO				5	3	3		14	V	エ		A		Ø	1			Reload Counter ENable Timer & Internet flip flop
ξ				-6	0	1							ĺ					flipflop
				7	D	3		0	u	T		C	M	T	2			·
				8	0	_												
				9	3	3		M	V	I		A	,_	5	5			Reload Timer O. both bytes.
SYSTEMS				A	5	5							_					both bytes.
SIS				В	D	3		0	u	T	·	T	Ţ	M	Ø			
- 1				С	1	4												
3		. ,		D	D	3		0	u	7		T	I	M	Ø			
COMPUTER				E	1	4.										- 1		
- 1				F	F	B .		3	I									Enable Interrusts
₹.	8	2	4-	0	C	q		Ŕ	E	T								Return
INTEGRATED		94.400c		1														
Z				2														